## Product Features

- $50-3000 \mathrm{MHz}$
- 13.5 dB Gain
- +26 dBm P1dB
- +37 dBm OIP3
- 2.0 dB Noise Figure
- MTTF > 100 years
- Lead-free/Green/RoHScompliant SOT-89 Package


## Product Description

The FP101 is a high dynamic range GaAs FET packaged in a low-cost surface-mount package. The combination of low noise figure and high output IP3 at the same bias point makes it ideal for receiver and transmitter applications. The FP101 achieves +37 dBm OIP3 with consistent quality to maintain MTTF values exceeding 100 years at mounting temperatures of $+85^{\circ} \mathrm{C}$ and is available in the environmentally-friendly lead-free/green/RoHS-compliant SOT-89 package.

All devices are $100 \%$ RF and DC tested. The product is targeted for applications where high linearity is required.

Functional Diagram


| Function | Pin No. |
| :---: | :---: |
| Input / Gate | 1 |
| Output / Drain | 3 |
| Ground | 2,4 |

## Specification

| DC Parameter | Units | Min | Tyo | Max | Comments |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Saturated Drain Current, $\mathrm{I}_{\text {dss }}$ Transconductance, $\mathrm{G}_{\mathrm{m}}$ Pinch Off Voltage, $\mathrm{V}_{\mathrm{p}}$ | $\begin{gathered} \mathrm{mA} \\ \mathrm{mS} \\ \mathrm{~V} \end{gathered}$ |  | $\begin{array}{r} 270 \\ 120 \\ -2.3 \\ \hline \end{array}$ |  | $\begin{aligned} & \mathrm{V}_{\mathrm{gs}}=0 \mathrm{~V}, \mathrm{~V}_{\mathrm{ds}}=3 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{ds}}=1.2 \mathrm{~mA} \end{aligned}$ |


| RF Parameter | Units | Min | Tyo | Max | Comments |
| :--- | :---: | :---: | :---: | :---: | :---: | :--- |
| Frequency Range | MHz | 50 | 800 | 3000 |  |
| Small Signal Gain, Gss | dB |  | 13.5 |  |  |
| Maximum Stable Gain, Gmsg | dB |  | 20.5 |  |  |
| Output P1dB | dBm | +23 | +26 |  |  |
| Output IP3 | dBm | +34 | +37 |  | $+8 \mathrm{dBm} /$ tone, 10 MHz spacing, 1850 MHz |
| Noise Figure | dB |  | 1.9 |  | $\mathrm{~V}_{\mathrm{ds}}=+5 \mathrm{~V}$ |

Test conditions unless otherwise noted: $\mathrm{T}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{ds}}=+8 \mathrm{~V}, \mathrm{I}_{\mathrm{dq}}=100 \mathrm{~mA}$, frequency $=800 \mathrm{MHz}$ in a 50 ohm system.

## Thermal Information

| Parameters | Rating |
| :--- | :--- |
| Operating Case Temperature | -40 to $+85^{\circ} \mathrm{C}$ |
| Storage Temperature | -55 to $+125^{\circ} \mathrm{C}$ |
| Thermal Resistance (junction to ground tab) | $68^{\circ} \mathrm{C} / \mathrm{W}$ |
| Junction Temperature $(8 \mathrm{~V} / 100 \mathrm{~mA})$ | $139^{\circ} \mathrm{C}$ |
| Junction Temperature ${ }^{*}(5 \mathrm{~V} / 100 \mathrm{~mA})$ | $119^{\circ} \mathrm{C}$ |

## Absolute Maximum Rating

| Parameter | Rating |
| :--- | :--- |
| Operating Case Temperature | -40 to $+85^{\circ} \mathrm{C}$ |
| Storage Temperature | -55 to $+150{ }^{\circ} \mathrm{C}$ |
| Gate to Source Voltage | -6 V |
| RF Input Power (continuous) | +17 dBm |
| DC Power | 2.0 W |
| Junction Temperature | $+220^{\circ} \mathrm{C}$ |

## Ordering Information

| Part No. | Description |
| :--- | :--- |
| FH101* | High Dynamic Range FET <br> (lead-tin SoT-89 package) |
| FH101-G | High Dynamic Range FET <br> (lead-freelgreen/RoHS-compliant SOT-89 package) |

[^0]*his package is being phased out in favor of the green package type which is backwards compatible for
existing designs. existing designs.

## Typical Device Data

S-Parameters $\left(\mathrm{V}_{\mathrm{ds}}=8 \mathrm{~V}, \mathrm{I}_{\mathrm{ds}}=100 \mathrm{~mA}, 25^{\circ} \mathrm{C}\right.$, Unmatched 50 ohm system $)$


## Reference Design (1800-1900 MHz)

Typical Performance

| Parameter | Value | Comments |
| :--- | :--- | :--- |
| Frequency | 1850 MHz |  |
| S21 - Gain | 13.9 dB |  |
| S11 - Input Return Loss | -23.6 dB |  |
| S22 - Output Return Loss | -13.5 dB |  |
| S12 - Isolation | -20.9 dB |  |
| Output IP3 | 36.2 dBm | See Note 1,3 |
| Output P1dB | 23.3 dBm | See Note 3 |
| Noise Figure | 3.6 dB |  |
| Drain Bias | $5 \mathrm{~V} @ 100 \mathrm{~mA}$ |  |

## Notes

1. OIP3 is measured with 2 tones at an output power of $+10 \mathrm{dBm} /$ tone with 10 MHz spacing at 1850 MHz . The suppression on the largest IM3 product is used to calculate OIP3 using a $2: 1$ slope rule. Test parameters were taken at $25^{\circ} \mathrm{C}$.
2. All components are 0603 size. Toko LL1608-FH chip inductors and AVX $\pm 0.1 \mathrm{pF}$ tolerance capacitors (C3 and C5) were used in the design. Other capacitor components are standard types. The overall circuit size should be minimized as much as possible.
3. The drain voltage can be increased to +8 V for increased output power performance (higher P1dB, higher OIP3). The gate voltage can be adjusted so that the drain bias can be anywhere between $50-150 \mathrm{~mA}$.


FP101 (SOT-89 Package) Mechanical Information
This package may contain lead-bearing materials. The plating material on the leads is SnPb

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Land Pattern

Produce harking
The FP101 wilnefmarked (A) it an 'FP101' designator white the Esteffree version, FP101-G be mane ed with an 'F101G' design for shown in trotline Drawing as 'YY (D YX'). ANNphanumeric lot code ('XXX') iss (TBa) marked below the part designer on hap surface of the package.
rape and rect pecifications for this part are 1 located Pone website in the "Application
Notes ing Notesizetion.

## 



Caution! ESD sensitive device.

ESD Rating: Class 1 C
Value: $\quad$ Passes $\geqslant 1000 \mathrm{~V}$ to $<2000 \mathrm{~V}$
Test: $\quad$ Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114
ESD Rating: Class IV
Value: $\quad$ Passes $\geqslant 1000$ V
Test: $\quad$ Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101
MSL Rating
FP101: Level 3 at $+235^{\circ} \mathrm{C}$ convection reflow FP101-G: Level 3 at $+260^{\circ} \mathrm{C}$ convection reflow Standard: JEDEC Standard J-STD-020

## Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35 mm (\#80 / . 0135 ") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz . Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

## FP101-G (Green / Lead-free SOT-89 Package) Mechanical Information

This package is lead-free/Green/RoHS-compliant. It is compatible with both lead-free (maximum $260^{\circ} \mathrm{C}$ reflow temperature) and leaded (maximum $245^{\circ} \mathrm{C}$ reflow temperature) soldering processes. The plating material on the leads is NiPdAu.

## Product Marking



Land Pattern


The FP101-G will be marked with an "F101G" designator. An alphanumeric lot code ("XXXX-X") is also marked below the part designator on the top surface of the package.
Tape and reel specifications for this part are located on the website in the "Application Notes" section.

## MSL / ESD Rating

Caution! ESD sensitive device.

ESD Rating: Class 1C

| Value: | Passes $\geqslant 1000$ V to $<2000 \mathrm{~V}$ |
| :--- | :--- |
| Test: | Human Body Model (HBM) |
| Standard: | JEDEC Standard JESD22-A114 |

ESD Rating: Class IV
Value: $\quad$ Passes $\geqslant 1000 \mathrm{~V}$ to $<2000 \mathrm{~V}$
Test: $\quad$ Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 3 at $+260^{\circ} \mathrm{C}$ convection reflow Standard: JEDEC Standard J-STD-020

## Mounting Config. Notes

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35 mm (\#80 / .0135") diameter drill and have a final plated thru diameter of $.25 \mathrm{~mm}\left(.010^{\prime \prime}\right)$.
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink
4. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
5. RF trace width depends upon the PC board material and construction.
6. Use 1 oz . Copper minimum.
7. All dimensions are in millimeters (inches). Angles are in degrees.

## Typical Device Data

S-Parameters $\left(\mathrm{V}_{\mathrm{D}}=+5 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=100 \mathrm{~mA}, \mathrm{~T}=25^{\circ} \mathrm{C}\right.$, calibrated to device leads)

| Freq (MHz) | S11 (dB) | S11 (ang) | S21 (dB) | S21 (ang) | S12 (dB) | S12 (ang) | S22 (dB) | S22 (ang) |
| :---: | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 200 | -0.05 | -11.65 | 13.09 | 170.35 | -40.11 | 83.52 | -20.18 | -20.22 |
| 400 | -0.03 | -23.12 | 13.00 | 161.72 | -33.94 | 77.88 | -18.83 | -41.57 |
| 600 | -0.18 | -36.31 | 12.87 | 151.32 | -30.39 | 68.68 | -19.57 | -59.31 |
| 800 | -0.32 | -47.17 | 12.65 | 142.63 | -28.11 | 61.81 | -18.20 | -76.47 |
| 1000 | -0.50 | -58.15 | 12.38 | 133.74 | -26.38 | 55.76 | -17.00 | -91.39 |
| 1200 | -0.67 | -69.49 | 12.09 | 125.22 | -25.12 | 48.54 | -16.25 | -103.87 |
| 1400 | -0.88 | -79.35 | 11.76 | 117.41 | -24.03 | 42.65 | -15.13 | -112.58 |
| 1600 | -0.99 | -89.35 | 11.43 | 109.46 | -23.28 | 36.62 | -14.26 | -121.97 |
| 1800 | -1.21 | -98.68 | 11.04 | 101.95 | -22.60 | 30.96 | -13.77 | -129.80 |
| 2000 | -1.33 | -107.48 | 10.68 | 94.92 | -21.97 | 25.56 | -13.13 | -136.00 |
| 2200 | -1.53 | -116.22 | 10.30 | 87.87 | -21.48 | 20.05 | -12.63 | -142.70 |
| 2400 | -1.67 | -124.67 | 9.94 | 81.13 | -21.06 | 14.86 | -12.13 | -148.50 |
| 2600 | -1.74 | -129.96 | 9.70 | 76.55 | -20.80 | 11.41 | -11.84 | -152.37 |
| 2800 | -1.87 | -137.82 | 9.34 | 70.28 | -20.44 | 6.62 | -11.55 | -157.82 |
| 3000 | -1.97 | -146.08 | 9.01 | 64.05 | -20.22 | 0.76 | -11.24 | -162.58 |

S-Parameters $\left(\mathrm{V}_{\mathrm{D}}=+8 \mathrm{~V}, \mathrm{I}_{\mathrm{D}}=100 \mathrm{~mA}, \mathrm{~T}=25^{\circ} \mathrm{C}\right.$, calibrated to device leads)

| Freq (MHz) | S11 (dB) | S11 (ang) | S21 (dB) | S21 (ang) | S12 (dB) | S12 (ang) | S22 (dB) | S22 (ang) |
| :---: | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 200 | -0.11 | -11.45 | 12.37 | 170.42 | -39.98 | 79.95 | -14.10 | -12.80 |
| 400 | -0.09 | -22.71 | 12.28 | 161.78 | -33.90 | 76.01 | -13.71 | -26.74 |
| 600 | -0.24 | -35.70 | 12.17 | 151.43 | -30.61 | 67.68 | -14.51 | -36.99 |
| 800 | -0.38 | -46.35 | 11.97 | 142.64 | -28.17 | 61.30 | -14.24 | -50.43 |
| 1000 | -0.53 | -57.07 | 11.72 | 133.73 | -26.47 | 54.53 | -14.01 | -63.83 |
| 1200 | -0.70 | -68.34 | 11.44 | 125.17 | -25.18 | 47.72 | -13.94 | -74.67 |
| 1400 | -0.90 | -77.99 | 11.13 | 117.20 | -24.20 | 41.43 | -13.43 | -85.29 |
| 1600 | -1.02 | -88.00 | 10.81 | 109.14 | -23.36 | 35.88 | -13.06 | -95.56 |
| 1800 | -1.24 | -97.21 | 10.43 | 101.55 | -22.67 | 30.53 | -12.84 | -104.03 |
| 2000 | -1.35 | -105.96 | 10.08 | 94.34 | -22.13 | 25.25 | -12.44 | -111.54 |
| 2200 | -1.54 | -114.67 | 9.70 | 87.18 | -21.60 | 20.06 | -12.16 | -119.40 |
| 2400 | -1.69 | -123.07 | 9.35 | 80.34 | -21.19 | 14.79 | -11.82 | -126.07 |
| 2600 | -1.76 | -128.30 | 9.11 | 75.57 | -20.96 | 11.26 | -11.63 | -130.63 |
| 2800 | -1.89 | -136.04 | 8.76 | 69.16 | -20.59 | 6.53 | -11.40 | -136.59 |
| 3000 | -2.00 | -144.31 | 8.43 | 62.87 | -20.35 | 1.69 | -11.16 | -141.99 |


[^0]:    Operation of this device above any of these parameters may cause permanent damage

